CLAIMS

What is claimed is:

1. A method of fabricating a MOS transistor, the method comprising:

creating a form structure above a starting structure, the form structure having an opening exposing a single portion of the starting structure;

forming a spacer in the opening of the form structure, the spacer extending over part of the starting structure along a sidewall of the form structure opening;

forming a semiconductor material in the opening of the form structure to create a formed semiconductor body having a single generally planar bottom surface above the starting structure;

removing the form structure and the spacer;

forming a gate structure disposed along at least a portion of a top and sides of the formed semiconductor body, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the formed semiconductor body; and

doping portions of the formed semiconductor body to form source/drains.

2. The method of claim 1, wherein the formed semiconductor body comprises a first body portion, a second body portion, and a third body portion, the second body portion being disposed between the first and third body portions and having first and second sides and a top, and wherein the gate structure is formed along at least a portion of the top and sides of the second body portion.

3. The method of claim 1, wherein forming the spacer comprises:

depositing a first spacer material layer over the form structure and over the exposed starting structure;

depositing a second spacer material layer over the first spacer material layer; and

etching the first and second spacer material layers, leaving a portion of the first spacer material layer extending over part of the starting structure along the sidewall of the form structure opening.

4. The method of claim 3, wherein the spacer is generally L-shaped.

5. The method of claim 4, wherein depositing the first spacer material layer comprises depositing silicon nitride over the form structure and over the exposed starting structure, and wherein depositing the second spacer material layer comprises depositing silicon dioxide over the first spacer material layer.

6. The method of claim 5, wherein removing the form structure and the spacer comprises wet etching the form structure and the spacer, leaving the formed semiconductor body having a single generally planar bottom surface above the starting structure.

7. The method of claim 3, wherein removing the form structure and the spacer comprises wet etching the form structure and the spacer, leaving the formed semiconductor body having a single generally planar bottom surface above the starting structure.

8. The method of claim 3, wherein the first and second spacer material layers are deposited using chemical vapor deposition or atomic layer deposition.

9. The method of claim 1, wherein forming the spacer comprises:

depositing a spacer material layer over the form structure and over the exposed starting structure; and

etching the spacer material layer to expose a portion of the starting structure, leaving a portion of the spacer material layer extending over part of the starting structure along the sidewall of the form structure opening.

10. The method of claim 9, wherein depositing the spacer material layer comprises depositing silicon nitride over the form structure and over the exposed starting structure.

11. The method of claim 9, wherein removing the form structure and the spacer comprises wet etching the form structure and the spacer, leaving the formed semiconductor body having a single generally planar bottom surface above the starting structure.

12. The method of claim 9, wherein the spacer material layer is deposited using chemical vapor deposition or atomic layer deposition.

13. A transistor, comprising:

a semiconductor body comprising first, second, and third body portions individually comprising a generally planar first bottom surface overlying a starting structure, the first and third body portions individually comprising doped source/drains, the second body portion comprising a top, first and second sides extending laterally between the first and third body portions, and a lithography independent width between the first and second sides; and

a gate structure disposed along at least a portion of the top and sides of the second body portion, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the second body portion.

14. The transistor of claim 13, wherein the first, second, and third body portions are disposed along an axis generally parallel to a plane of the starting structure.

15. The transistor of claim 13, wherein the starting structure comprises a semiconductor and wherein the semiconductor body comprises silicon, silicon germanium, germanium, or gallium arsenide.

16. The transistor of claim 13, wherein the semiconductor body comprises epitaxial silicon.

17. The transistor of claim 13, wherein the gate structure comprises a lateral gate length, and wherein the lithography independent width of the second body portion is less than the lateral gate length of the gate structure.

18. The transistor of claim 17, wherein the gate length is about 25 nm or less.

19. The transistor of claim 17, wherein the second body portion comprises a depth between the top and the generally planar bottom surface, and wherein the depth of the second body portion and the gate length are generally equal.

20. The transistor of claim 13, wherein the second body portion comprises a second bottom surface spaced from the starting structure, and wherein the gate structure is disposed along at least a portion of the second bottom surface between the second body portion and the starting structure.

21. The transistor of claim 20, wherein the gate structure comprises a lateral gate length, and wherein the lithography independent width of the second body portion is less than the lateral gate length of the gate structure.

22. The transistor of claim 13, wherein the gate structure comprises a lateral gate length, and wherein the lithography independent width of the second body portion is less than one half of the lateral gate length of the gate structure.

23. The transistor of claim 22, wherein the lithography independent width of the second body portion is about one third of the lateral gate length of the gate structure.

24. A transistor, comprising:

a semiconductor body comprising first, second, and third body portions individually comprising a generally planar first bottom surface overlying a semiconductor starting structure, the first and third body portions individually comprising doped source/drains, the second body portion comprising a second bottom surface spaced from the starting structure, first and second sides extending laterally between the first and third body portions, and a top; and

a gate structure disposed along at least a portion of the top and sides of the second body portion and along at least a portion of the second bottom surface between the second body portion and the starting structure, the gate structure comprising a conductive gate electrode and a gate dielectric disposed between the gate electrode and the second body portion.

25. The transistor of claim 24, wherein the first, second, and third body portions are disposed along an axis generally parallel to a plane of the starting structure.

26. The transistor of claim 24, wherein the semiconductor body comprises silicon, silicon germanium, germanium, or gallium arsenide.

27. The transistor of claim 24, wherein the gate structure comprises a lateral gate length, and wherein the lithography independent width of the second body portion is less than the lateral gate length of the gate structure.

28. The transistor of claim 24, wherein the gate structure comprises a lateral gate length, and wherein second body portion comprises a width between the first and second less than one half of the lateral gate length.

29. The transistor of claim 24, wherein the width of the second body portion is about one third of the lateral gate length.